Appl. No.

09/764,711

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AMENDMENTS TO THE CLAIMS

33. (Currently Amended) An integrated capacitor formed in a trench having a width of no more than about $0.25\ 0.18\ \mu m$ and a depth of greater than about $10\ \mu m$ an aspect ratio greater than about 20:1, comprising:

a dielectric layer lining the trench; and a conductively doped, as-deposited polysilicon layer filling the trench.

- 34. (Original) The integrated capacitor of Claim 33, wherein the conductively doped polysilicon layer comprises arsenic.
- 35. (Original) The integrated capacitor of Claim 33, wherein the trench has a depth of greater than about 5 μ m.
- 36. (Original) The integrated capacitor of Claim 35, wherein the trench has a depth of greater than about 7 μ m.
- 37. (Original) The integrated capacitor of Claim 36, wherein the trench is formed in a semiconductor substrate.

Please added the following claim:

38. (New) An integrated capacitor formed in trench having a width of no more than about 0.25 μ m and an aspect ratio of about 40:1, comprising:

a dielectric layer lining the trench; and a conductively doped, as-deposited polysilicon layer filling the trench.